UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/899,157	07/06/2001	Masanari Asano	107317-00030	2825

4372 7590 09/22/2005

ARENT FOX PLLC
1050 CONNECTICUT AVENUE, N.W.
SUITE 400
WASHINGTON, DC 20036

EXAMINER	
SINGH, DALIP K	

ART UNIT	PAPER NUMBER
2671	

DATE MAILED: 09/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/899,157	ASANO, MASANARI	
	Examiner	Art Unit	
	Dalip K. Singh	2671	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☑ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☑ All b)☐ Some * c)☐ None of:

1.☑ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 3, 5, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,351,291 B1 to Asano in view of U.S. Patent No. 6,351,292 B1 to Knox et al.

a. Regarding claim 1, Asano **discloses** an image memory (frame memory 4, Fig. 1)(...video data A for one frame of main images (or background images) on the display are stored in an area 10. and on-screen-display...stored in an area 11...col. 3, lines 5-16); a display buffer memory (display buffer memory 6, Fig. 1)(...the frame controller 5 reads data selectively from the video data area 10 or the OSD data area in the frame memory 4...and writes the line image data into the display buffer memory 6...line image data is read from the display buffer memory 6 and outputted to the monitor 7...col. 3, lines 16-29); and a control section (frame controller 5, Fig. 1)(...on a screen of the monitor 7 are displayed a movie image...as a main image (a background image) and a small still image of flowers as an on-screen-display (OSD) image 13...the OSD image 13 is a square image with a small frame...col. 3, lines 35-46). Asano **does not disclose** said control section including a data expansion control section capable of increasing a data amount of the second image data group read from said image memory (frame memory 4). Knox et al. **discloses** line doubling mode wherein OSD data is repeated such that each OSD line is repeated (...the function bits contain a single bit to indicate whether the "Line Doubling Mode" is enabled...the OSD unit will repeat the OSD data such that each OSD line is

repeated...col. 5, lines 30-41). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify Asano with the feature "line doubling mode where each OSD line is repeated" as taught by Knox et al. **because** it reduces the OSD bitstream size to be reduced resulting in lower bandwidth requirements.

b. Regarding claims 2 and 3, Asano **does not disclose** data expansion control section including a magnification control for magnifying the OSD data. Knox et al. **discloses** OSD data magnification utilizing the "line doubling mode" (col. 5, lines 30-67). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify Asano with the feature "line doubling mode where each OSD line is repeated" as taught by Knox et al. **because** it reduces the OSD bitstream size to be reduced resulting in lower bandwidth requirements.

c. Regarding claim 5, Asano **discloses** a display buffer memory (display buffer memory 6, Fig. 1)(...the frame controller 5 reads data selectively from the video data area 10 or the OSD data area in the frame memory 4...and writes the line image data into the display buffer memory 6...line image data is read from the display buffer memory 6 and outputted to the monitor 7...col. 3, lines 16-29).

d. Regarding claim 17, it is similar in scope to claim 1 above and is rejected under the same rationale.

e. Regarding claim 18, it is similar in scope to claim 3 above and is rejected under the same rationale.

3. Claims 4 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,351,291 B1 to Asano in view of U.S. Patent No. 6,351,292 B1 to Knox et al. as applied to claim 1 above, and further in view of U.S. Patent No. 5,926,174 to Shibamiya et al.

a. Regarding claim 4, Asano-Knox combination **is silent about** wherein magnification control section adds a new data group obtained by conducting a linear interpolation for the second image data group to the second image data group. Shibamiya et al. **discloses** OSD (on-screen display) operations for displaying necessary information on the display unit 15 for facilitating various adjustments by the operator making use of interpolation circuit 125 (...the linear interpolation...the image data of the interpolated pixel is determined from the image data of the pixels on both sides of the interpolated pixel...col. 14, lines 20-30...the OSD data 118 is enlarged in a doubled size...the data is then enlarged into a doubled size...by the interpolation circuit 125...col. 23, lines 60-67; col. 24, lines 1-60). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made modify Asano-Knox combination with the feature "linear interpolation for OSD data" as taught by Shibamiya et al. **because** it provides a more flexible OSD data display with different font size selection as per user input.

b. Regarding claim 19, it is similar in scope to claim 4 above and is rejected under the same rationale.

2. Claims 6,7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,351,291 B1 to Asano in view of U.S. Patent No. 6,351,292 B1 to Knox et al. as applied to claim 1 above, and further in view of U.S. Patent No. 6,215,4674 to Suga et al.

a. Regarding claims 6, 7 and 9, Asano-Knox combination **does not disclose** wherein the first image data group (...first image data group...for a background) is magnified using a circuit included in the magnification control section. Suga et al. **discloses** a display control having a plurality of different display modes, and where OSD data is displayed according to different font sizes, shapes (...appropriately display OSD data in correspondence with display states with different image

resolutions...driving conditions differences in various display modes can be absorbed, and the OSD data can be stably displayed...OSD data having a font size...corresponding to the enlarged or reduced size is used to maintain a desired size and shape...a plurality of types of image signals corresponding to different resolutions...OSD display operations matching the respective display modes can be attained...col. 1, lines 50-67; col. 2, lines 5-41). Suga et al. **discloses** background image being capable of being magnified as well as the OSD image (...processing in the case of 640 dots...as one display mode of a VGA...the horizontal...pixel period is sampled 1,280 times to enlarge the horizontal dots to 1,280 dots...2-line enlargement is performed...800 dots...VESA standard...col. 16, lines 1-60...Figs. 26A and 26B which show control for enlarging the character size in the display control apparatus...col. 19, lines 4-10; lines 45-60). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify the Asano-Knox combination with the feature "OSD-Background image magnification capabilities" as taught by Suga et al. **because** it provides for a more flexible display arrangement of background and OSD data.

3. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,351,291 B1 to Asano in view of U.S. Patent No. 6,351,292 B1 to Knox et al. as applied to claim 1 above, and further in view of U.S. Patent No. 5,926,174 to Shibamiya et al., and further in view of U.S. Patent No. 6,215,4674 to Suga et al.

a. Regarding claim 8, Asano-Knox-Shibamiya combination **does not disclose** wherein the first image data group (...first image data group...for a background) is magnified using a circuit included in the magnification control section. Suga et al. **discloses** a display control having a plurality of different display modes, and where OSD data is displayed according to different font sizes, shapes (...appropriately display OSD data in correspondence with display states with different image

resolutions...driving conditions differences in various display modes can be absorbed, and the OSD data can be stably displayed...OSD data having a font size...corresponding to the enlarged or reduced size is used to maintain a desired size and shape...a plurality of types of image signals corresponding to different resolutions...OSD display operations matching the respective display modes can be attained...col. 1, lines 50-67; col. 2, lines 5-41). Suga et al. **discloses** background image being capable of being magnified as well as the OSD image (...processing in the case of 640 dots...as one display mode of a VGA...the horizontal...pixel period is sampled 1,280 times to enlarge the horizontal dots to 1,280 dots...2-line enlargement is performed...800 dots...VESA standard...col. 16, lines 1-60...Figs. 26A and 26B which show control for enlarging the character size in the display control apparatus...col. 19, lines 4-10; lines 45-60). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify the Asano-Knox- Shibamiya combination with the feature "OSD-Background image magnification capabilities" as taught by Suga et al. **because** it provides for a more flexible display arrangement of background and OSD data.

4. Claims 10, 11 and 12-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,351,291 B1 to Asano in view of U.S. Patent No. 6,351,292 B1 to Knox et al. as applied to claim 1 above, and further in view of U.S. Patent No. 5,489,947 to Cooper.

a. Regarding claims 10 and 11, Asano-Knox combination **is silent about** a bit conversion to increase a number of bits of the second image data group i.e., OSD data. Cooper **discloses** OSD display unit 1509-9 converting the four-bit graphic image component representative words to eight-bit words by adding four binary "0s" as the least four significant bits to the four-bit words thereby increasing a number of bits of the second image data group (OSD data)(...converts the four-bit...words to eight-bit words...by adding four binary "0s" as the least four significant bits to the four-bit

words...col. 6, lines 50-67); storage of such converted data into display buffer memory (frame store section 1513-1-5, Fig. 2; ...frame store section 1513-1-5 for storing frames of video information during the decoding and decompression operation...col. 5, lines 5-15). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify Asano-Knox combination with the feature "bit conversion and adding of 0s to low-order bits" as taught by Cooper **because** it provides an efficient way to insert a graphic image into a video image (col. 7, lines 20-26).

b. Regarding claim 12, Asano-Knox combination **is silent about** adding data "0" to low-order bits of the second image data group. Cooper **discloses** OSD display unit 1509-9 converting the four-bit graphic image component representative words to eight-bit words by adding four binary "0s" as the least four significant bits to the four-bit words thereby increasing a number of bits of the second image data group (OSD data)(...converts the four-bit...words to eight-bit words...by adding four binary "0s" as the least four significant bits to the four-bit words...col. 6, lines 50-67); storage of such converted data into display buffer memory (frame store section 1513-1-5, Fig. 2; ...frame store section 1513-1-5 for storing frames of video information during the decoding and decompression operation...col. 5, lines 5-15); and second processing of smoothing processing to substantially equalize difference between data obtained from the first processing (...the video image...groups correspond to two pixels...the 4:2:0 image...groups are converted to...by interpolation within video display unit 1509-5...col. 5, lines 40-61). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify Asano-Knox combination with the feature "bit conversion and adding of "0s" to low-order bits and interpolation" as taught by Cooper **because** it provides an efficient way to insert a graphic image into a video image (col. 7, lines 20-26).

c. Regarding claim 13, Asano-Cox combination **is silent about** display information table containing display information items; address information items; OSD display position specifying information to specify a display position on the display screen. Cooper **discloses** graphic image component representative words being stored in OSD section 1513-3 of RAM 1513 (..words are stored..in components groups as is indicated in the table in the form of a header for the bit map...OSD display unit 1509-9 requests data from OSD section 1513-3 via memory controller 1509-3 as required...col. 6, lines 43-65). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify Asano-Cox combination with the feature "graphic image words being stored in OSD memory area" as taught by Cooper **because** it simplifies storage of components for video images and graphics images as it simplifies the OSD arrangement by avoiding the need for conversion from one set of components to another (col. 6, lines 10-21).

d. Regarding claim 14, Cooper **discloses use** of a FIFO buffer memory 1509-1 working in tandem with RAM 1513. FIFO buffer memory can be written to and read from repetitively thus being rewritable.

e. Regarding claims 15 and 16, they are similar in scope to claim 13 above and are rejected under the same rationale.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Dalip K. Singh** whose telephone number is **(571) 272-7792**. The examiner can normally be reached on Mon-Friday (10:30AM-6: 30PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Ulka Chauhan**, can be reached at **(571) 272-7782**.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, please contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). Please note that the new Central Official FAX number for application specific communications with the USPTO is **571-273-8300** (effective July 15, 2005).

Dalip K. Singh
Examiner, Art Unit 2671

dks
September 12, 2005

ULKA J. CHAUHAN
PRIMARY EXAMINER